Abstracts

Analysis of Interconnection Delay on Very High-Speed LSI/VLSI Chips Using an MIS Microstrip Line Model

H. Hasegawa and S. Seki. "Analysis of Interconnection Delay on Very High-Speed LSI/VLSI Chips Using an MIS Microstrip Line Model." 1984 Transactions on Microwave Theory and Techniques 32.12 (Dec. 1984 [T-MTT] (1984 Symposium Issue)): 1721-1727.

Using an MIS (metal-insulator-semiconductor) microstrip-line model for interconnection and its equivalent circuit representation, on-chip interconnection delay in very high-speed LSI/VLSI's is analyzed in the time domain, changing interconnection geometry, substrate resistivity, and terminal conditions. The results show the following 1) the "lumped capacitance" approximation is inapplicable for interconnections in very high-speed LSI/VLSI's (t/sub pd/ of below 100-200 ps); 2) as compared to the semi-insulating substrate, the presence of the slow-wave mode and mode transition in the semiconducting substrates causes 1.5-2 times increase in the delay time and 2-10 times increase in the rise time and 3) in order to realize propagation delay times of less than 100 ps per gate at LSI/VLSI levels, the effective signal source resistance of the gate should be less than 500 Omega so as to long interconnections.

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